REMARKS

This application was originally filed on 2 June 1998 with ten claims, two of which were written in independent form. No claims have been allowed.

Claims 1-10 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,222,515 to Yamaguchi et al. ("Yamaguchi"). The applicant respectfully disagrees.

"A person shall be entitled to a patent unless," creates an initial presumption of patentability in favor of the applicant. 35 U.S.C. § 102. "We think the precise language of 35 U.S.C. § 102 that, "a person shall be entitled to a patent unless," concerning novelty and unobviousness, clearly places a burden of proof on the Patent Office which requires it to produce the factual basis for its rejection of an application under sections 102 and 103, see Graham and Adams." In re Warner, 379 F.2d 1011, 1016 (C.C.P.A. 1967) (referencing Graham v. John Deere Co., 383 U.S. 1 (1966) and United States v. Adams, 383 U.S. 39 (1966)). "As adapted to ex parte procedure, Graham is interpreted as continuing to place the 'burden of proof on the Patent Office which requires it to produce the factual basis for its rejection of an application under sections 102 and 103'." In re Piasecki, 745 F.2d 1468 (Fed. Cir. 1984) (citing In re Warner, 379 F.2d at 1016).

"The prima facie case is a procedural tool which, as used in patent examination (as by courts in general), means not only that the evidence of the prior art would reasonably allow the conclusion the examiner seeks, but also that the prior art compels such a conclusion if the applicant produces no evidence or argument to rebut it." *In re Spada*, 911 F.2d 705, 708 n.3 (Fed. Cir. 1990).

The applicant respectfully submits the Examiner has failed to meet the burden of proof required to establish a *prima facie* case of anticipation. Section 2131 of the Manual of Patent Examiner's Procedure provides:

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described in a single prior art reference." Verdegaal Bros. v. Union Oil Co. Of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053, (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as contained in the . . . claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

TI-25995 - Page 2



The elements must be arranged as in the claim under review. In re Bond, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990).

With respect to independent Claim 1, the Examiner has failed to point to any teaching in Yamaguchi that reasonably suggests "offsetting a first pixel value a first predetermined amount to form a first offset pixel value and displaying said first offset pixel value during a first display frame; and offsetting said first pixel value by the opposite of said first predetermined amount to form a second offset pixel value and displaying said second offset pixel value during a second display frame, such that the average of said displayed first offset pixel value and said second offset pixel value is said first pixel value" as recited by Claim 1.

With respect to independent Claim 6, the Examiner has failed to point to any teaching in Yamaguchi that reasonably suggests "a logic circuit offsetting a first pixel value a first predetermined amount to form a first offset pixel value, said logic circuit also offsetting said first said pixel value by the opposite of said first predetermined amount to form a second offset pixel value; and display means displaying said first offset pixel value during a first display frame and displaying said second offset pixel value during a second display frame, such that the average of said displayed first offset pixel value and said second offset pixel value is said first pixel value" as recited by Claim 6.

The Examiner stated, "As to claims 1 and 6, Yamaguchi et al teaches a system of displaying a digital video data associated with a method comprising a logic circuit offsetting a first pixel value a first predetermined amount (2V, 4V) to form a first offset pixel value, said logic circuit (4) also offsetting said first said pixel value by the opposite of said first predetermined amount (-2V, -4V) to form a second offset value; and display panel (19) displaying said first offset pixel value during a first display frame 'a positive frame' and displaying said second offset pixel value during a second display frame 'a negative frame', such that the average of said displayed first offset pixel value and said second offset pixel value is said first pixel value 'said means effective voltage of (+/- 3V) is shown by hatching in figure 7B' (see figures 1A, 1B, 7B, column 5, lines 58-64 and column 8, lines 11-27)."

The Examiner has failed to make a reasonable attempt to read the teachings of the prior art onto the limitations of the claims presented and therefore has failed to establish a prima facie

TI-25995 - Page 3

case of anticipation. For example, the Examiner has not stated what value in Yamaguchi is a "first pixel value" and therefore the Examiner's attempts to read Yamaguchi onto the present claim flounder. Having not established a first pixel value, the Examiner states a first predetermined offset amount is (2V, 4V) and a second predetermined offset amount is (-2V, -4V). These each appear to the applicant to be two amounts and the Examiner offers no explanation or support for his interpretation of Yamaguchi. The Examiner then states the average of said displayed first offset pixel value and said second offset pixel value is +/- 3V. The applicant respectfully submits, that if the Examiner is averaging 2V, 4V, -2V, and -4V the average would be 0 volts. The Examiner's interpretation of Yamaguchi clearly is unsupported by Yamaguchi and does not follow the clear teachings of Yamaguchi. For example, Yamaguchi states, "To realize a gray-scale level 3, 6 (V) is applied to the first field and 2 (V) to the second field to produce a mean effective voltage of 4 (V) for one frame." (col. 8, lines 23-25).

These passages cited by the Examiner simply do not support the Examiner's transformation of the teachings of Yamaguchi to the recited elements of Claims 1 and 6, nor is there any basis or suggestion in the prior art to support this novel interpretation of the prior art. The Examiner's rejection is unsupported by the prior art, fails to establish a prima facie case of anticipation, and therefore should be withdrawn.

Claims 2-5 and 7-10 depend from Claims 1 and 6 and should be deemed allowable for that reason and on their own merits. For the reasons argued above with respect to Claims 1 and 6, the Examiner has failed to present a prima facie case of anticipation and the rejections therefore should be withdrawn.

In view of the amendments and the remarks presented herewith, it is believed that the claims currently in the application accord with the requirements of 35 U.S.C. § 112 and are allowable over the prior art of record. Therefore, it is urged that the pending claims are in condition for allowance. Reconsideration of the present application is respectfully requested.

Respectfully submitted,

Charles A. Brill

Reg. No. 37,786

Texas Instruments Incorporated PO Box 655474 M/S 3999 Dallas, TX 75265 (972) 917-4379

FAX: (972) 917-4418